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Customer No. 24498
Serial No. 10/511,654

Docket No. PU020122

Amendments to the claims:

1. (Previously presented) An apparatus for processing a received signal containing a datastream, comprising:

a signal decoder, the signal decoder generating a first error signal in response to indecipherable data received by the decoder; and

a transport processor, the transport processor receiving the first error signal, the transport processor generating a second error signal after receiving the first error signal.

2. (Original) The apparatus of claim 1, wherein the datastream comprises a modulated signal containing data packets.

3. (Previously presented) The apparatus of claim 2, further comprising:

a transport bus, the transport bus forwarding data packets to subsequent processing stages; and

at least one synchronization signal, the transport processor generating the second error signal in response to receiving the synchronization signal.

4. (Previously presented) The apparatus of claim 3, wherein the second error signal is forwarded to the transport bus so as to have a synchronized relationship to the data packets being forwarded via the transport bus.

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5. (Previously presented) The apparatus of claim 3, wherein the second error signal is formed as a series of logical high frames, each logical high frame being associated with a data packet.

6. (Currently amended) The apparatus of claim 5, wherein the duration of each logical high frame of the second error signal has a duration greater than the data packet associated with the logical high frame.

7. (Previously presented) The apparatus of claim 5, wherein each logical high frame of the second error signal begins at an earlier time than the data packet associated with the logical high frame.

8. (Previously presented) The apparatus of claim 5, wherein each logical high frame of the second error signal ends at a later time than the data packet associated with the logical high frame.

9. (Previously presented) The apparatus of claim 3, further comprising a demodulator, the demodulator deriving the synchronization signal from the received signal.

10. (Previously presented) The apparatus of claim 1 wherein the transport processor is implemented as a microprocessor.

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11. (Previously presented) A system for generating an error signal based on an error encountered while processing a received signal which includes an image representative datastream containing data packets, comprising:

a forward error detecting and correcting decoder which generates a first error signal;

a synchronization signal derived from the received signal;

a transport processor interconnected to receive the first error signal and the synchronization signal, the transport processor generating a second error signal in response to the first error signal and the synchronization signal.

12. (Previously presented) The system of claim 11, further comprising a transport bus, the data packets being forwarded to subsequent processing stages via the transport bus.

13. (Previously presented) The system of claim 12, wherein the second error signal is forwarded via the transport bus simultaneously with the data packets associated with the second error signal.

14. (Previously presented) The system of claim 13, wherein the data packets are forwarded as a series of discrete spaced apart frames, the second error signal being adapted to indicate an error in a defective data packet by having a duration that spans the frame of the defective data packet.

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15. (Previously presented) The system of claim 14, wherein the second error signal assumes a logical low state when no error is present in a data packet.

16. (Previously presented) The system of claim 15, wherein the forward error detecting and correcting decoder is a Reed-Solomon decoder.

17. (Previously presented) The system of claim 11 wherein the transport processor is implemented as a microprocessor.

18. (Previously presented) A method for processing a received signal containing an image representative datastream containing data packets, the method comprising the steps of:
demodulating the received signal to produce a demodulated signal;
error detecting the demodulated signal to produce a first error signal;
forwarding the first error signal to a transport processor;
forwarding a synchronization signal to the transport processor, thereby associating the first error signal with a particular data packet; and
generating a second error signal in response to the synchronization signal being received by the transport processor.

19. (Currently amended) A method according to claim 17 claim 18, further comprising the step of generating the second error signal as a series of discrete frames, each frame having a duration greater than an associated data packet.

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20. (Original) A method according to claim 18, further comprising the steps of:
starting each discrete second error signal frame before an associated data packet begins;
and

stopping each discrete second error signal frame after an associated data packet ends.

21. (Original) A method according to claim 19, wherein the error detecting step
comprises Reed-Solomon error detection and correction.

22. (New) An apparatus for processing a received signal containing a datastream,
comprising:

a signal decoder, the signal decoder generating a first error signal in response to
indecipherable data received by the decoder; and

a transport processor, the transport processor receiving the first error signal, the
transport processor generating a second error signal after receiving the first error signal,

wherein the second error signal is formed as a series of logical high frames, each
logical high frame being associated with a data packet,

wherein each logical high frame of the second error signal begins at an earlier time than
the data packet associated with the logical high frame, and

wherein each logical high frame of the second error signal begins at an earlier time than
the data packet associated with the logical high frame.